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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,374	10/30/2001	Gayvin E. Stong	10010660-1	2639

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EXAMINER
KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,374	STONG ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,8-12 and 26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,8-12 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This is a FINAL OFFICE ACTION in response to Amendment filed 6/9/2005.

Claims 2-6, 8-12, 26-32 are pending.

Response to Arguments

Applicant's arguments filed 6/9/2005 have been fully considered but they are not persuasive.

Regarding Claim 26, Applicant contends that the "transition and capacitively coupled faults", disclosed by Lepejian patent and as cited in the Office Action, are not equivalent to the faults caused by stimulation of non-deterministic operations as taught in the present Specification. In response to Applicant's argument, based on Applicant's own definition of non-deterministic operations to be "contention conditions that would not occur during actual operation of the IC" described on page 2, lines 9-10 and page 6, lines 15-26 of the present specification, the Examiner notes that Lepejian's "transition and capacitively coupled faults" are random unpredictable faults that are not detected that appear only at normal speed operation. Further, in the Background of the Invention, Lepejian cites conventional approaches with their drawbacks in resolving the "coupled faults" problem. However, Lepejian, recognizes in fact, if the word were to contain an even number of transition or capacitive coupling faults which cause the bit to read the opposite of the intended data, even the presence of the faults is masked. Finally, in the Summary of the Invention, Lepejian discloses, "testing the memories at

full speed reduces both test time and cost and improves the quality of the testing by providing the ability of detecting transition and capacitively coupled faults", by generating the address locally at each memory with a pseudo-random generator based on a clocked shift register with linear feedback defined by a primitive polynomial, thus minimizing the routing area devoted to address lines used in accessing the embedded memories. Therefore, Lepejian discloses testing "transition and capacitively coupled faults", which corresponds to a non-deterministic operation, (Lepejian, col. 3, 4 and lines 50-67 and 1-20).

Furthermore, the limitation of "non-deterministic operation" is recited in the preamble and not in the main body of the claim, and as such the recitation has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Applicant argues, page 8, that the claimed feature of "the test enable signals logically combine with the control lines" does not correspond to combining the encoded data on bus 86 with mode control 11 in the de-skewing circuit 70 as disclosed by Lepejian. In response to Applicant's argument, as shown in Figures 1, 3 and 4, data, address and control signals are provided to the de-skewing circuit 70, which logically

combines and synchronizes, by employing synchronously clocked latches 72 and 73 to provide the de-skewing function, as is common practice in VLSI design. An additional logic element, AND gate 71, inhibits the writing of test data to invalid address locations, Figure 4. Therefore, Applicant's broadly recited feature of "logically combining" encompasses the equivalent logical function of the de-skewing circuit 70, as taught by Lepejian.

The rejection of claims 2-6, 8-12, 26-32 over the prior art under 35 USC § 102 as being anticipated by Lepejian et al, and Claim 30 under 35 USC § 103 as being unpatentable over Lepejian et al. in view of Powell et al., is still maintained, as set forth in the prior Office Action, which is presented herewith in its entirety, below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-6, 8-12, 26-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Lepejian et al. (U.S. Patent No. 5,974,579), issued: October 26, 1999.

Regarding independent Claims 26 and 31, Lepejian discloses an apparatus and a method, for a built-in self- test (BIST) circuit for testing one or more embedded memories (memory array 90) in an integrated circuit, Abstract, Figure 1. The memory

element having at least one deterministic operation corresponding to a "pass/fail testing" the memories at full speed by writing data to each memory address, reading it back out, and then comparing the input and output data and reporting the results in a pass/fail format on test output. Further, the memory element having at least one non-deterministic operation corresponds to testing the memories at full speed by providing the ability of detecting "transition and capacitive coupled faults", see Summary of the Invention, (Col. 3, lines 58-61). Based on Applicant's definition of the non-deterministic operation, described in the Applicant's Background of the invention, as a BIST result of simultaneous read and write, thereby rendering the test unusable, the Examiner notes that the "transition and capacitive coupled faults", as disclosed by Lepejian, are equivalent to the faults caused by non-deterministic operation, the apparatus comprising:

A code generator, comprising an Encoded Data Generator (50) and a Pattern Counter (22) accepting seed input from the Main Finite State Machine (20) in response to a clock signal (29) and using the Encoded Data Generator (50) for encoding a test code (encoded data 12), Figure 6.

A decoder (85) accepts the test codes (encoded data 12) and remaps (decodes) the encoded data from the main controller 10 and provides test enable signals (decoded data) on lines (86) having at least two lines corresponding to at least two test enable signals. Furthermore, Lepejian discloses de-skewing circuit 70, which logically combines the test enable signals (decoded data) on lines (86) with the control lines from MODE CONTROL 11, which in turn generates Decoded Data and Control, and

passes the control and the decoded data to the memory under test 90, Figure 1 to stimulate only deterministic operations when in a test enabled condition (Test Mode On via Mode Control), using BIST methodology JTAG standards, wherein the test mode disables the normal operation of the circuit and enables BIST.

Regarding Claims 2, 9, Lepejian discloses a code generator, comprising a counter (Pattern Counter 22) and an Encoded Data Generator (50), for generating a test code, Figure 6. Furthermore, the Abstract describes with respect to the claim feature of generating sequential numbers, "the BIST circuit includes one or more data generators for supplying a sequence of data to be written to the various addresses of each memory".

Regarding Claims 3, 8, Lepejian discloses a pseudo-random address generator 40 based on a synchronous shift register with linear feedback which permits generation of the pseudo-random sequence of "0's" and "1's" that is shifted through the shift register, and which can be implemented in a code generator for generating a test code of pseudo-random patterns, Figure 2.

Regarding Claim 4, Lepejian discloses a memory element (memory array 90) comprising multiple ports, such as Decoded Data (86) input data to the memory and Data out (82) output data from the memory, Figure 1.

Regarding Claims 5, 6, Lepejian discloses wherein when in (Test Mode On via Mode Control), the decoder (85) maps each test code value (encoded data 12) to a unique state such as logic level "1" or "0" at the output lines (86) and maps more than one test code value (encoded data 12).

Regarding Claim 10, Lepejian discloses driving all test enable signals to a constant value when in a test code disable condition, such as when the decoder (data decoder 85) is in a decode disabled condition (Test Mode "Off" via Mode Control) such as during the operational mode, the output lines (86) reflect a value that when combined with the respective memory access lines located between de-skewing circuit 70 and memory array 90, Figure 1, the test mode enables all possible Read /Write memory operations.

Regarding Claim 11, Lepejian discloses mapping a value of each test code to a unique state of the test enable signals, such as when in a decode enabled condition (Test Mode On via Mode Control), the output lines (86) are responsive to the test code (encoded data 12) and reflect a value on the output lines (86) that when combined with respective memory access lines located between de-skewing circuit 70 and memory array 90, Figure 1, the test mode disables the non-deterministic operations, such as detecting "transition and capacitive coupled faults" occurring during read / write operations. Then, address filter 50 responds to the pseudo-random sequence of addresses so as to lock out only those illegal addresses from the smaller address space, by generating an "ADRR HALT" signal 52 when the address space of the second (smaller) memory 91 has been exceeded, Figure 1.

Regarding Claim 12, Lepejian discloses using decoder 85 for mapping the encoded data 12 and providing test enable signals (decoded data) on lines (86).

Regarding Claim 27, Lepejian discloses at lest two different memory elements (90 and 91, Figure 1), each memory element associated with an Encoded Data Generator (50) and a decoder (85).

Regarding Claims 28, 29, Lepejian discloses wherein one of the non-deterministic operations is a multiple write operation and a simultaneous read and write, corresponding to testing the memories at full speed by providing the ability of detecting "transition and capacitive coupled faults", see Summary of the Invention (Col. 3, lines 58-61). Based on Applicant's definition of the non-deterministic operation, described in the Applicant's Background of the invention, as a BIST result of simultaneous read and write, thereby rendering the test unusable, the Examiner notes that the "transition and capacitive coupled faults", as disclosed by Lepejian, are equivalent to the faults caused by non-deterministic operation.

Regarding Claim 32, Lepejian discloses comparing a resulting test signature (output data 82) with a known good test signature (input data 81) using data comparator (80) which compares the output data 82 from embedded memory 90 with the corresponding input data 81 and reports the results in a pass/fail format on test output line 19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

> to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lepejian et al. (U.S. Patent No. 5,974,579) in view of Powell et al. (U.S. Patent No. 6,014,336, issued: January 11, 2000).

Regarding Claim 30, Lepejian substantially discloses the claimed invention as applied to independent claim 26, above. Lepejian does not explicitly disclose wherein the "decoder is a look up table implemented in read only memory".

However, Powell et al. (U.S. Patent No. 6,014,336) discloses built-in self-tests for memory systems including a Read only Memory decoder 70, which receives binary signals from program counter 66 via a bus 68, decoded by the ROM address decoder 70. For a person skilled in the art, ROM is commonly used as a lookup table.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ a Read only Memory decoder as taught by Powell in the built-in self test (BIST) circuit of Lepejian for the purpose of testing embedded memory arrays, since a Read only Memory provides design flexibility in implementing decoding functions, by using software programming thus avoiding cumbersome hardware logic normally associated with decoding design.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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By: _____

Date: 28 July 2005
Office Action: Final Rejection

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